FIG. 1 prior art

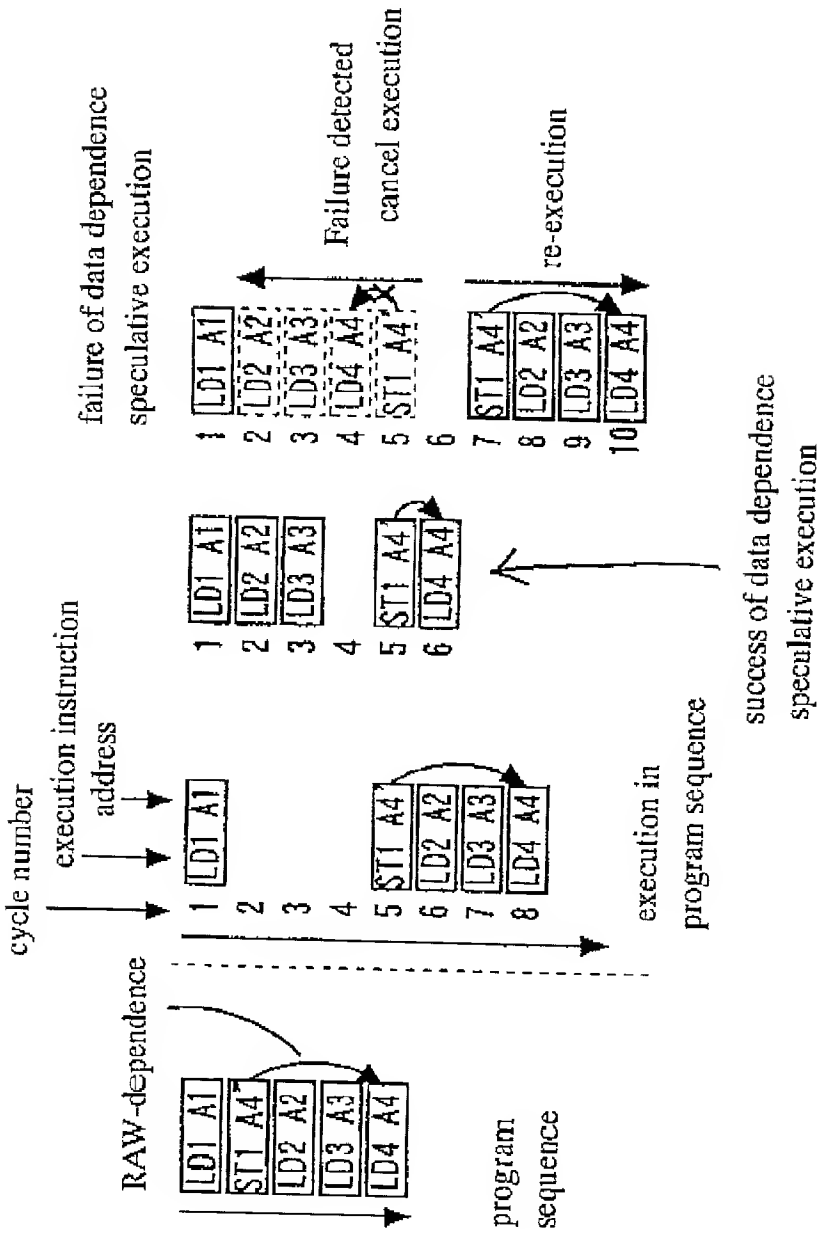


FIG. 2 prior art

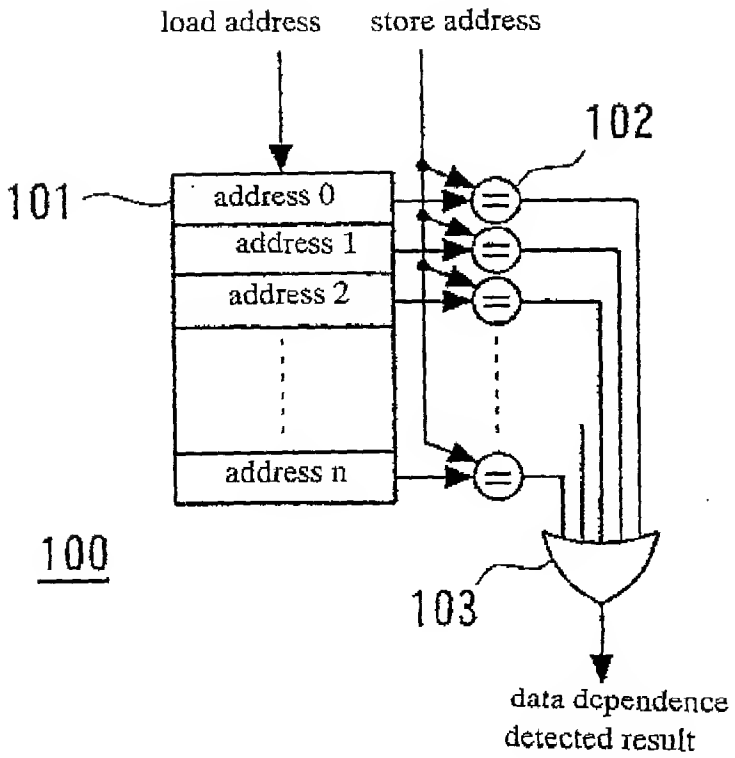


FIG. 3

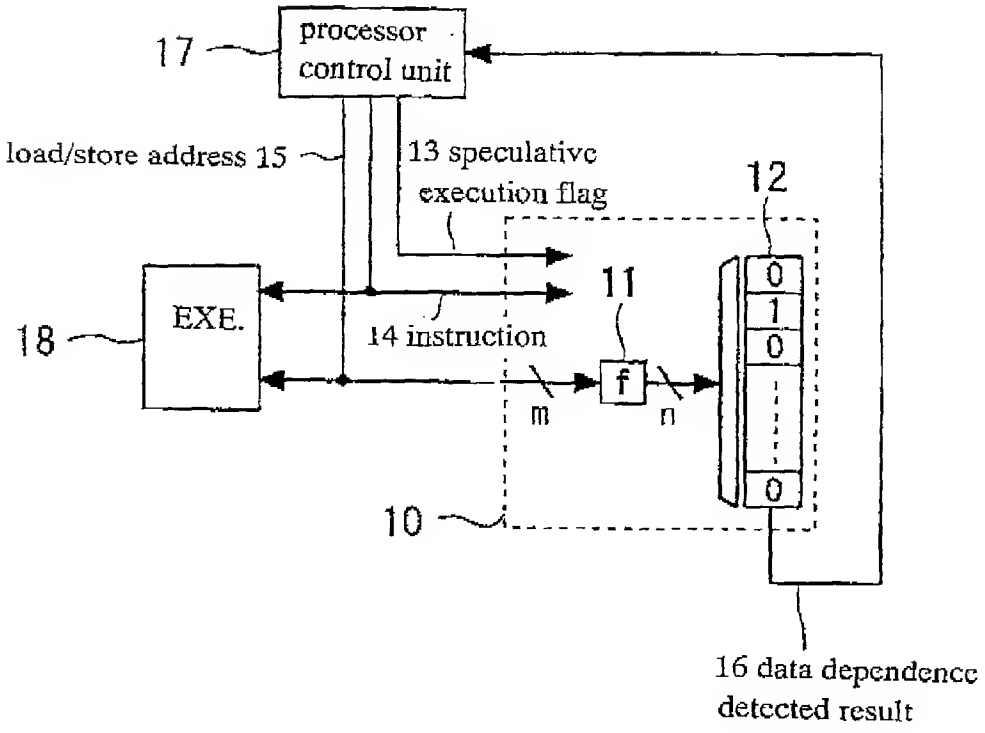

17
processor control unit
load/store address 15
13 speculative execution flag
12
11
18
EXE.
14 instruction
f
m
n
0
1
0
0
10
16 data dependence detected result

FIG. 4

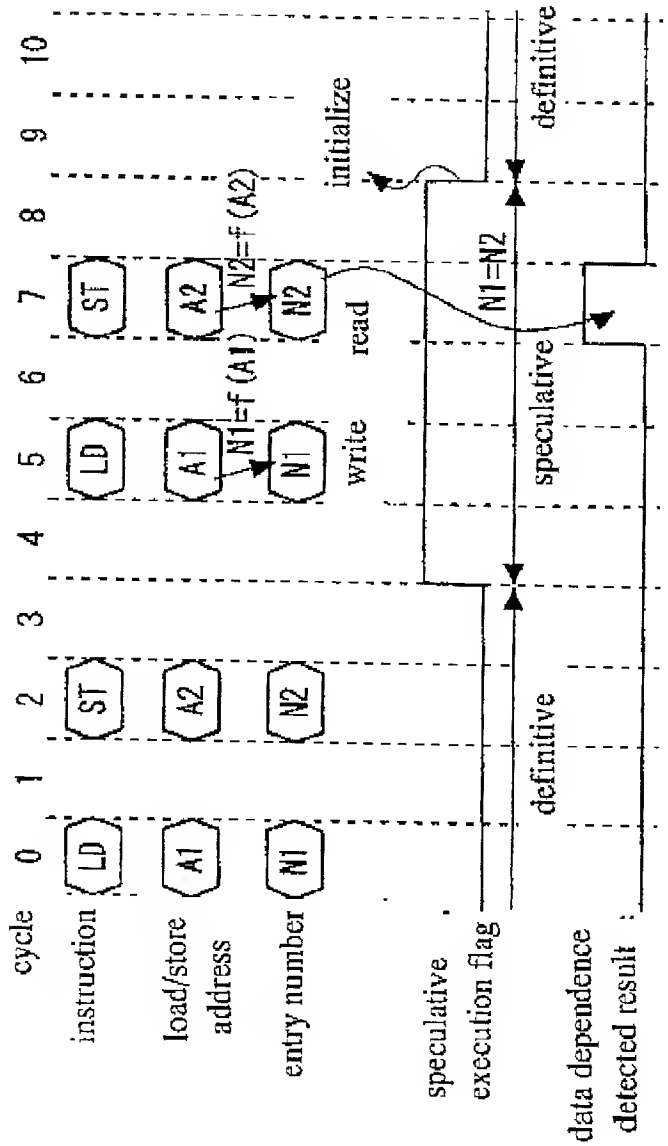

cycle
instruction
load/store address
entry number
speculative execution flag
data dependence detected result
LD
ST
A1
A2
N1
N2
N1=f (A1)
N2=f (A2)
write
read
initialize
N1=N2
speculative
definitive
definitive

FIG. 5

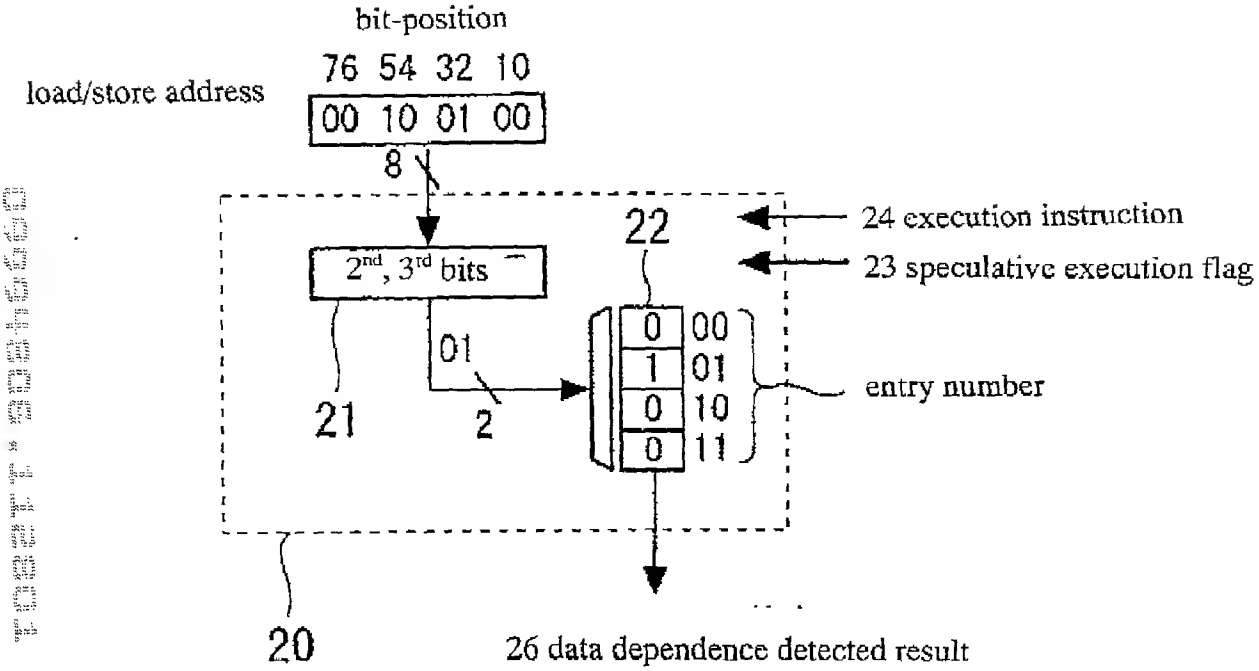

bit-position
76 54 32 10
load/store address
00 10 01 00
8
2nd, 3rd bits
01
21
2
22
24 execution instruction
23 speculative execution flag
0 00
1 01
0 10
0 11
entry number
20
26 data dependence detected result

FIG. 6A

FIG. 6B

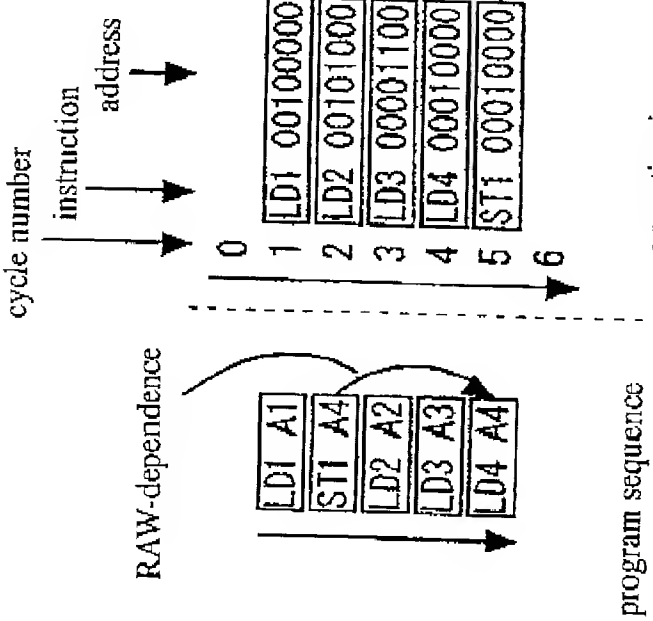


FIG. 6C

FIG. 7A

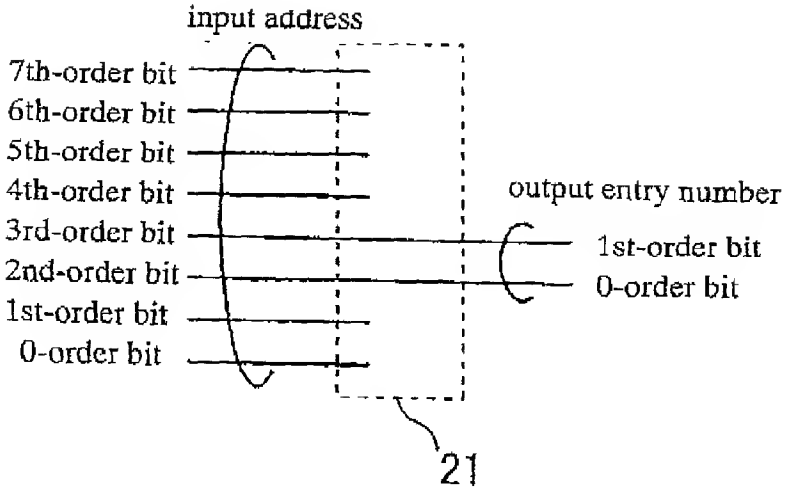

input address
7th-order bit
6th-order bit
5th-order bit
4th-order bit
3rd-order bit
2nd-order bit
1st-order bit
0-order bit
output entry number
1st-order bit
0-order bit
21

FIG. 7B

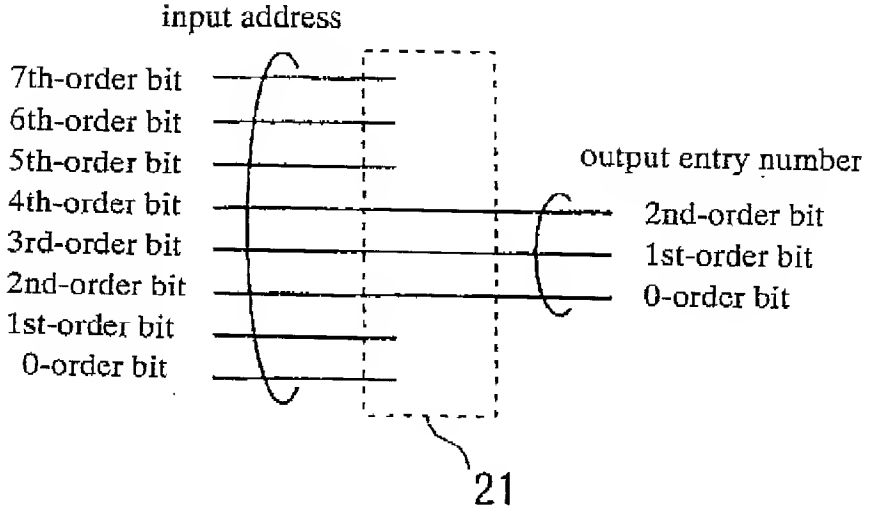

input address
7th-order bit
6th-order bit
5th-order bit
4th-order bit
3rd-order bit
2nd-order bit
1st-order bit
0-order bit
output entry number
2nd-order bit
1st-order bit
0-order bit
21

FIG. 7C

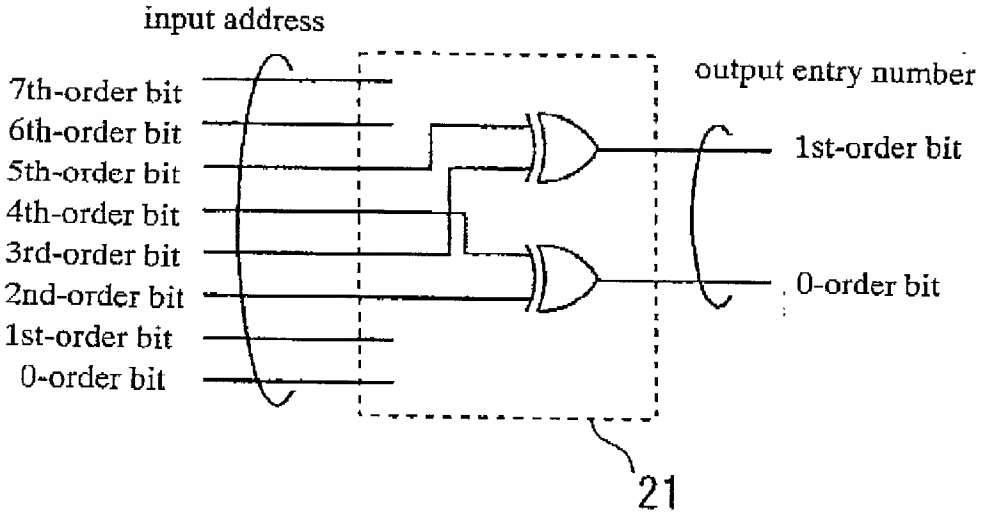

input address
7th-order bit
6th-order bit
5th-order bit
4th-order bit
3rd-order bit
2nd-order bit
1st-order bit
0-order bit
output entry number
1st-order bit
0-order bit
21

FIG. 8

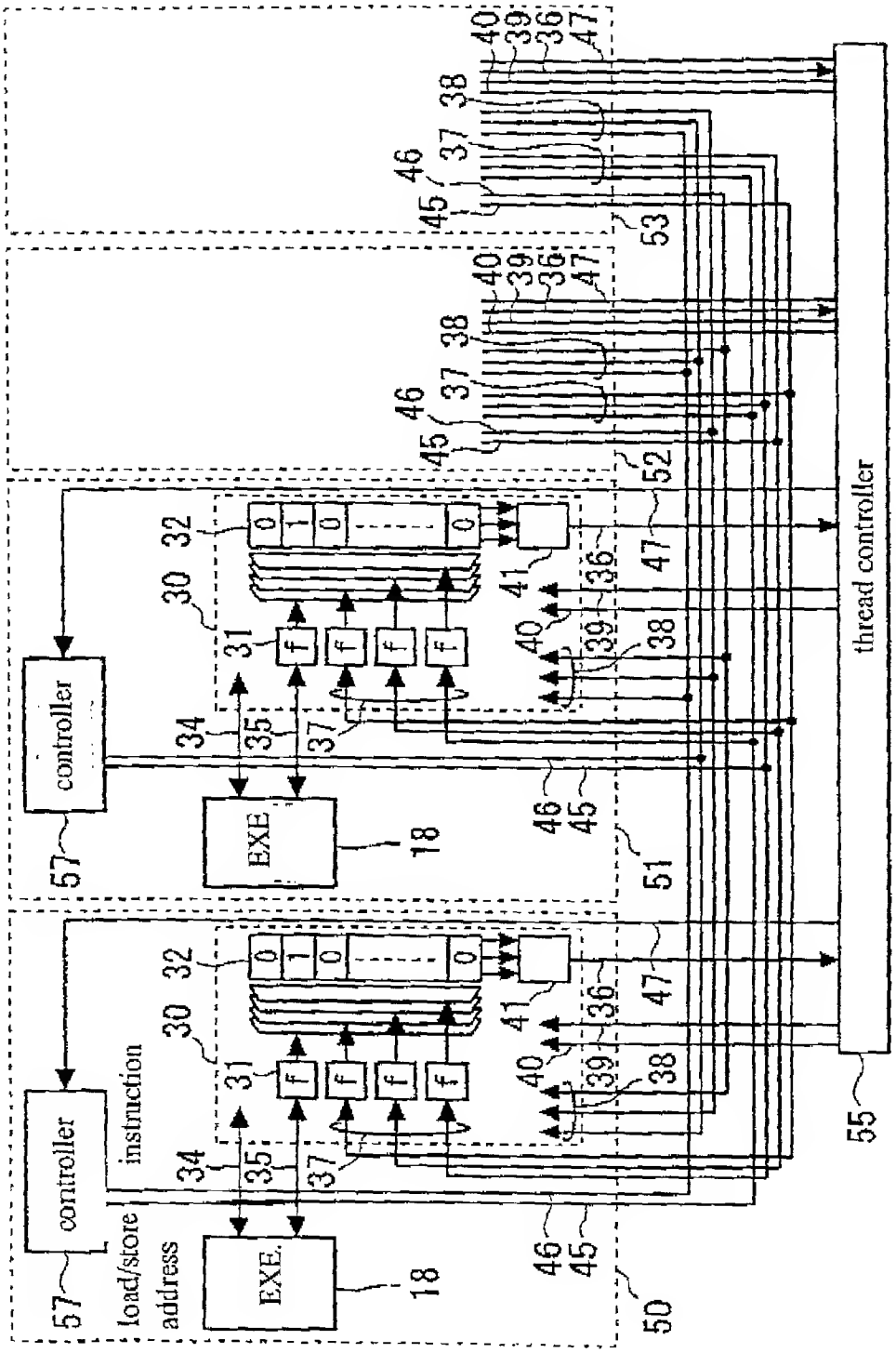

thread controller
controller
instruction
load/store
address
EXE
EXE.
18
30
31
32
34
35
36
37
38
39
40
41
45
46
47
50
51
52
53
55
57
f
0
1

FIG. 9A

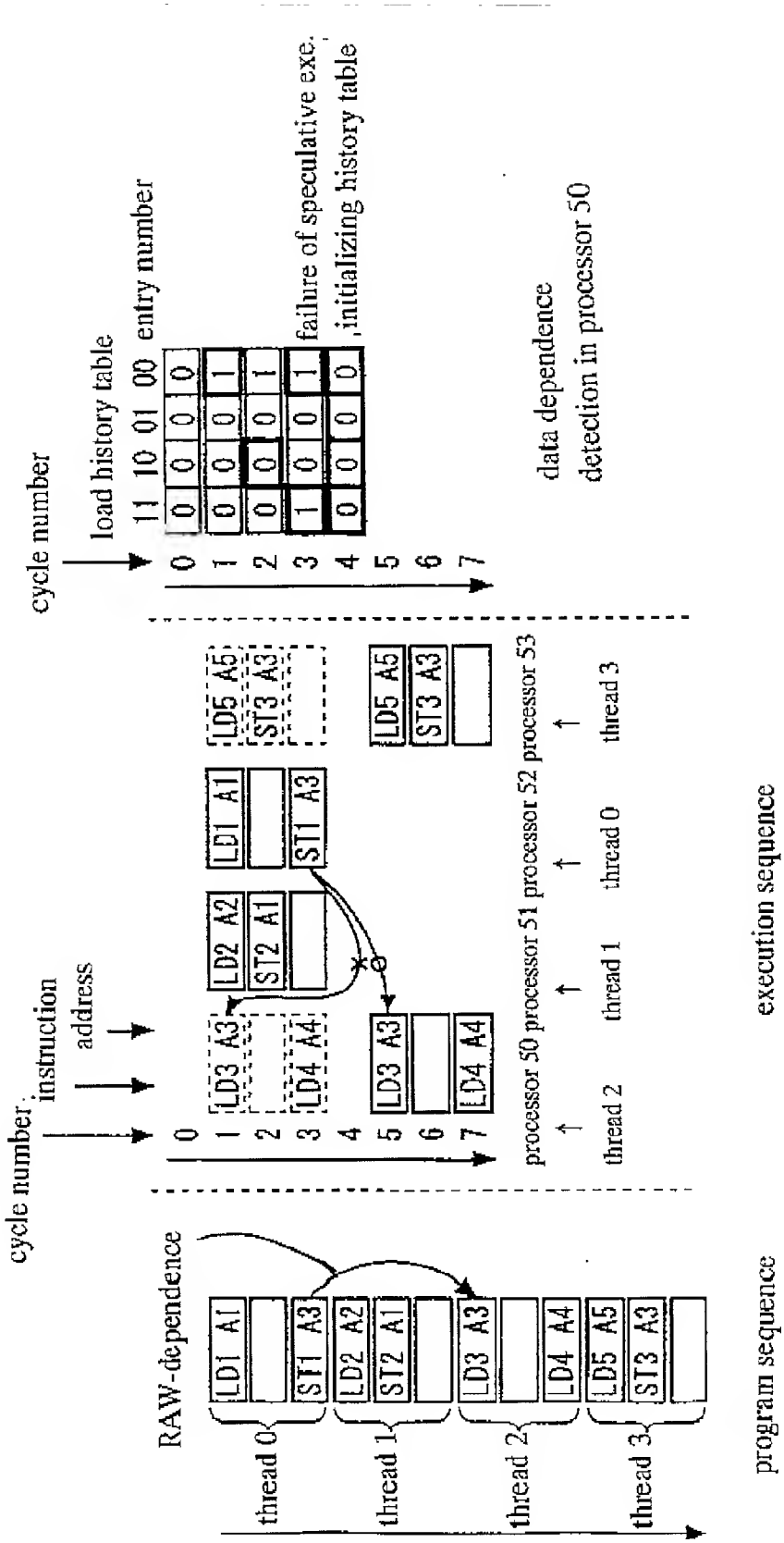
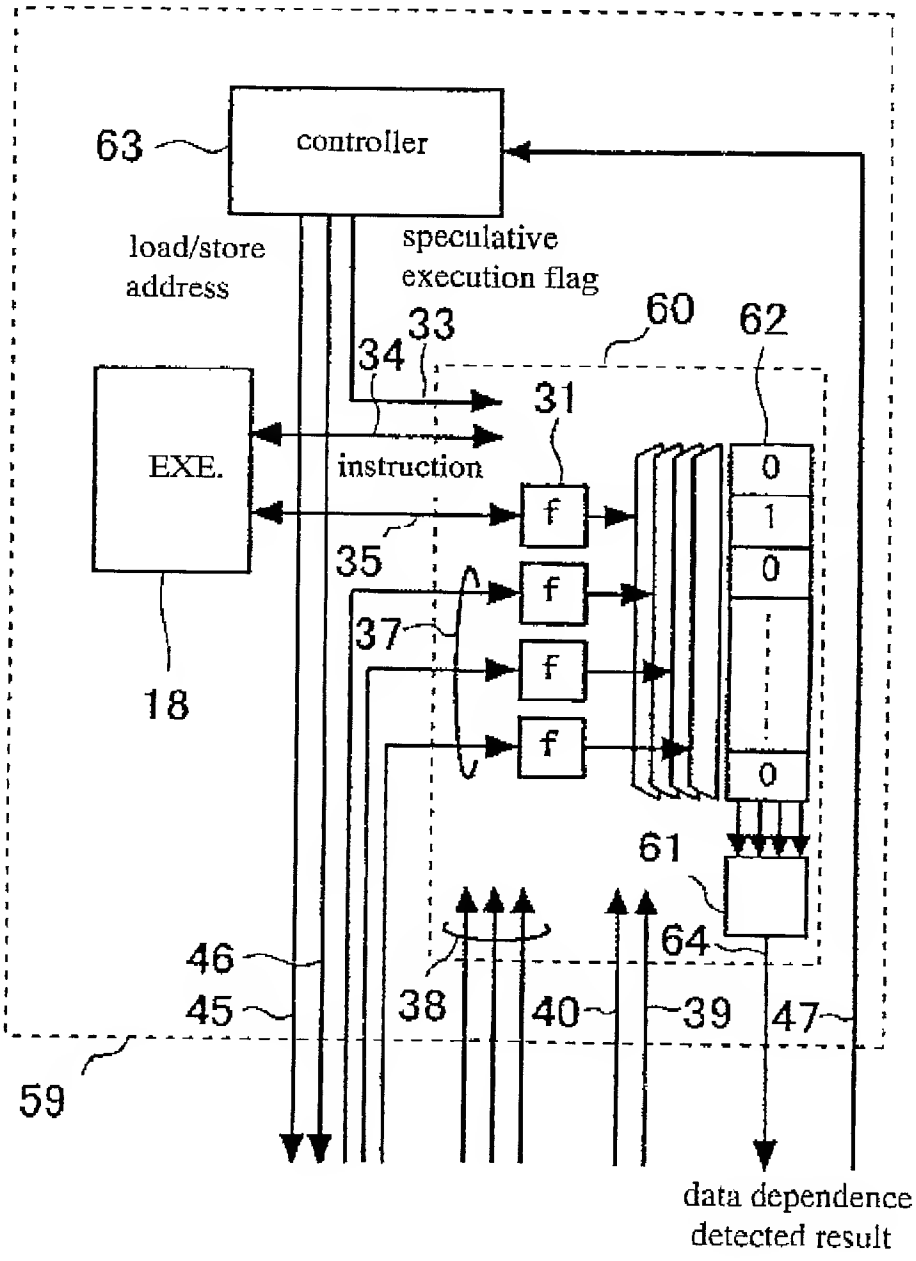


FIG. 9B

FIG. 9C

FIG. 10


63
controller
load/store address
speculative execution flag
33
34
60
62
31
EXE.
instruction
18
35
37
f
f
f
f
0
1
0
0
61
64
46
45
38
40
39
47
59
data dependence detected result